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~~(b) By using the gate array platform given in Fig. 1.30, implement the CMOS circuit as compactly as possible with the aspect ratio, which is the ratio of vertical dimension to horizontal dimension, as close to 1 as possible. Solution Manual for CMOS Digital Integrated Circuits Analysis and Design 4th Edition by Kang~~

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~~The power supply voltage is 1.2V, and the output load capacitance is 10fF. (a) Calculate the rise time and the fall time of the output signal using the exact method (differential equation) and average current method. 6.10Consider a CMOS inverter with the following parameters: VT0,n= 0.5V nCox= 98 A/V2(W/L)n= 20~~

~~Solved-> 6.10 Consider a CMOS inverter from Chapter 6---~~

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~~Solved-> 6.2Consider switching delays for 40 fF in a from---~~

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